# PATENT COOPERATION TREATY

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**INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY**
(Chapter II of the Patent Cooperation Treaty)
(PCT Article 36 and Rule 70)

| Applicant's or agent's file reference PEB383 | FOR FURTHER ACTION | See Form PCT/IPEA/416 |
|---|---|---|
| International application No. PCT/JP2004/005637 | International filing date *(day/month/year)* 20.04.2004 | Priority date *(day/month/year)* 22.04.2003 |
| International Patent Classification (IPC) or national classification and IPC Int.Cl.[7] H01L21/3205, 21/304, 21/306 | | |
| Applicant EBARA CORPORATION | | |

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 4 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☑ a total of 6 sheets, as follows:
      ☑ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ a total of (indicate type and number of electronic carrier(s)) _____, containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:
   - ☑ Box No. I Basis of the report
   - ☐ Box No. II Priority
   - ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - ☐ Box No. IV Lack of unity of invention
   - ☑ Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - ☐ Box No. VI Certain documents cited
   - ☐ Box No. VII Certain defects in the international application
   - ☐ Box No. VIII Certain observations on the international application

| Date of submission of the demand | Date of completion of this report |
|---|---|
| 18.11.2004 | 25.07.2005 |
| Name and mailing address of the IPEA/JP<br>**Japan Patent Office**<br>3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan | Authorized officer 4L 3239<br>TAKASHI WATAHIKI<br>Telephone No. +81-3-3581-1101 Ext. 3498 |

**INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY**

International application No.
PCT/JP2004/005637

**Box No. I Basis of the report**

1. With regard to the language, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ This report is based on translations from the original language into the following language _____ , which is the language of a translation furnished for the purposes of:

- ☐ international search (under Rules 12.3 and 23.1(b))
- ☐ publication of the international application (under Rule 12.4)
- ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the elements of the international application, this report is based on (*replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report):*

☐ the international application as originally filed/furnished

☑ the description:

pages 1-136 as originally filed/furnished
pages* _____ received by this Authority on _____
pages* _____ received by this Authority on _____

☑ the claims:

pages 139-142 as originally filed/furnished
pages* _____ as amended (together with any statement) under Article 19
pages* 137,138,143-146 received by this Authority on 18.11.2004
pages* _____ received by this Authority on _____

☑ the drawings:

pages 1/46-46/46 as originally filed/furnished
pages* _____ received by this Authority on _____
pages* _____ received by this Authority on _____

☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing.

3. ☑ The amendments have resulted in the cancellation of:

- ☐ the description, pages _____
- ☑ the claims, Nos. 35,39
- ☐ the drawings , sheets/figs _____
- ☐ the sequence listing (specify): _____
- ☐ any table(s) related to sequence listing (specify): _____

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

- ☐ the description, pages _____
- ☐ the claims, Nos. _____
- ☐ the drawings, sheets/figs _____
- ☐ the sequence listing (specify): _____
- ☐ any table(s) related to sequence listing (specify): _____

* *If item 4 applies, some or all of those sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP2004/005637

**Box No. V** Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

| | | | |
|---|---|---|---|
| Novelty (N) | Claims | 1-28,32,40,41 | YES |
| | Claims | 29-31,33,34,36-38 | NO |
| Inventive step (IS) | Claims | 1-28,40,41 | YES |
| | Claims | 29-34,36-38 | NO |
| Industrial applicability (IA) | Claims | 1-34,36-38,40,41 | YES |
| | Claims | | NO |

2. Citations and explanations(Rule 70.7)

D1:JP 2002-353223 A(SONY CORPORATION) 2002.12.06
D2:JP 2001-144050 A(HITACHI CHEMICAL CO., LTD.) 2001.05.25
D3:JP 10-214834 A(MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD) 1998.08.11
D4:JP 2001-284297 A(SONY CORPORATION) 2001.10.12
D5:EP 001278241 A2(MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD)2003.01.22
(The document D1,D2 and D4 was not cited in the international search report.)

[Claims 29-31,33,34,38]
The subject matter of claims 29-31,33,34,38 does not appear to be novel and to involve an inventive step with respect to D1.
"Barrier metal 4" and "copper interconnect layer 6" in D1 correspond to "the interconnect material" in the invention in claim 29.

[Claims 29-31,33,34,36,37]
The subject matter of claims 29-31,33,34,36,37 does not appear to be novel and to involve an inventive step with respect to D2.

[Claim 32]
The subject matter of claim 32 does not appear to involve an inventive step with respect to D1,D2.
The subject matter of claim 32 is a well-known technology.

[Claim 38]
The subject matter of claim 38 does not appear to involve an inventive step with respect to D3,D4.
D4(See[0011]) discloses that low pressure polish can prevent a defect.
Therefore,in the invention in D3,the person skilled in the art would easily apply low pressure polishing in the second polishing step.

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of: Box No.V, item2

[Claims 29-34,36,37]
The subject matter of claims 29-34,36,37 does not appear to involve an inventive step with respect to D4,D5.
In D5,the second stage of the CMP performed with high pressure enables high polishing rate.
On the other hand, D4(See[0011]) discloses that high pressure polishing enables high polishing rate but it causes defect.
Therefore, in the invention in D5,performing low pressure polishing in the latter phase of the second stage of the CMP, in consideration of prevention of a defect,a person skilled in the art can do it easily.

[Claims 1-28,40,41]
The subject matter of claims 1-28,40,41 are neither disclosed in any of the documents cited in the ISR nor obvious to a person skilled in the art.

CLAIMS

1. (Amended) A substrate processing method for removing unnecessary interconnect material and barrier material on a substrate and flattening a surface of the substrate, wherein said interconnect material is embedded in interconnect recesses, said interconnect recesses being formed on a surface of an insulating material and having a film of said barrier material formed on the surface of an insulating material, said method comprising:

eliminating a level difference in the surface of the interconnect material to flatten the surface;

removing the interconnect material until the interconnect material present in the non-interconnect region of the substrate becomes a thin film or remains partly on the barrier material while applying a first pressure to the substrate;

removing the interconnect material in the form of the thin film or remaining partly on the barrier material while applying a second pressure, which is lower than the first pressure, to the substrate, thereby exposing the barrier material or further processing the barrier material;

simultaneously removing the unnecessary interconnect material and the barrier material until the barrier material present in the non-interconnect region becomes a thin film or remains partly while applying a third pressure to the substrate; and

removing the unnecessary interconnect material and the barrier material present in the non-interconnect region while applying a fourth pressure, which is lower than the third pressure, to the substrate, thereby exposing the insulating material in the non-interconnect region or further processing the insulating material.

2. The substrate processing method according to claim 1 further comprising simultaneously removing the unnecessary interconnect material, the barrier material and the insulating material.

3. (Amended) A substrate processing method for removing unnecessary interconnect material and barrier material on a substrate and flattening a surface of the substrate, wherein said interconnect material is embedded in interconnect recesses, said interconnect recesses being formed on a surface of an insulating material and having a film of said barrier material formed on the surface of an insulating material, said method comprising:

a first step of eliminating a level difference in the surface of the interconnect material to flatten the surface;

a second step of removing the interconnect material until the interconnect material present in the non-interconnect region of the substrate becomes a thin film or remains partly on the barrier material while applying a first pressure to the substrate;

a third step of removing the interconnect material in the form of the thin film or remaining partly on the barrier material while applying a second pressure, which is lower than the first pressure, to the substrate, thereby exposing the barrier material or further processing the barrier material;

a fourth step of simultaneously removing the unnecessary interconnect material and the barrier material until the barrier material present in the non-interconnect region becomes a thin film or remains partly while applying a third pressure to the substrate; and

a fifth step of removing the unnecessary interconnect material and the barrier material present in the non-interconnect region while applying a fourth pressure, which is lower than the third pressure, to the substrate, thereby exposing the insulating material in the non-interconnect region or further processing the insulating material.

4. The substrate processing method according to claim 3 further comprising a sixth step of simultaneously removing the unnecessary interconnect material, the barrier material and the insulating material.

5. The substrate processing method according to claim 1 or 3, wherein the step of eliminating a level difference in the surface of the interconnect material to flatten the surface is carried out by cutting or grinding.

29. (Amended) A substrate processing method for removing unnecessary interconnect material and barrier material on a substrate and flattening a surface of the substrate, wherein said interconnect material is embedded in interconnect recesses, said interconnect recesses being formed on a surface of an insulating material and having a film of said barrier material formed on the surface of an insulating material, said method comprising:

removing the interconnect material until the interconnect material present in the non-interconnect region of the substrate becomes a thin film or remains partly while applying a first pressure to the substrate; and then

completely removing the interconnect material, present in the non-interconnect region, in the form of the thin film or remaining partly while applying a second pressure, which is lower than the first pressure, to the substrate, thereby exposing an underlying material present under the interconnect material in the non-interconnect region.

30. The substrate processing method according to claim 29, wherein the step of removing the interconnect material until the interconnect material present in the non-interconnect region of the substrate becomes a thin film or remains partly comprises an additional step of eliminating a level difference in the surface of the interconnect material.

31. The substrate processing method according to claim 29, wherein the step of removing the interconnect material until the interconnect material present in the non-interconnect region of the substrate becomes a thin film or remains partly is terminated when the film thickness of the interconnect material present in the non-interconnect region has reached a value of not more than 300 nm.

32. (Amended) The substrate processing method according to claim 31, wherein the film thickness of the interconnect material present in the non-interconnect region is detected with an eddy current-type or optical film thickness measuring means.

33. The substrate processing method according to claim 29, wherein the processing rate of the interconnect material in the step of completely removing the interconnect material, present in the non-interconnect region, in the form of the thin film or remaining partly is lower than the processing rate of the interconnect material in the step of removing the interconnect material until the interconnect material present in the non-interconnect region of the substrate becomes a thin film or remains partly.

34. The substrate processing method according to claim 29, wherein the step of completely removing the interconnect material, present in the non-interconnect region, in the form of the thin film or remaining partly is carried out by using a processing liquid or a chemical liquid.

35. (Cancelled)

36. The substrate processing method according to claim 29 further comprising removing the underlying material present in the non-interconnect region until a material present under the underlying material becomes exposed.

37. The substrate processing method according to claim 36, wherein the step of removing the underlying material comprises a step of removing the underlying material until the underlying material becomes a thin film or remains partly, and a step of removing the underlying material in the non-interconnect region until the material present under the underlying material becomes exposed.

38. (Amended) A substrate processing method for removing unnecessary interconnect material and barrier material on a substrate and flattening a surface of the substrate, wherein said interconnect material is embedded in interconnect recesses, said interconnect recesses being formed on a surface of an insulating material and having a film of said barrier material formed on the surface of an insulating material, said method comprising:

simultaneously removing the unnecessary interconnect material and barrier material until the barrier material present in the non-interconnect region of the substrate becomes a thin film or remains partly while applying a first pressure to the substrate; and then

removing the unnecessary interconnect material and the barrier material in the form of the thin film or remaining partly while applying a second pressure, which is lower than the first pressure to the substrate, thereby exposing an underlying material present under the barrier material in the non-interconnect region.

39. (Cancelled)

40. (Amended) A substrate processing apparatus for performing the substrate processing method according to claim 1, comprising:

an electrolytic processing section, provided with an end point detection device, for carrying out electrolytic processing of a substrate held by a substrate holder;

a CMP section, provided with an end point detection device, for carrying out chemical mechanical polishing of the substrate held by a substrate holder; and

a substrate transfer device for transferring the substrate;

wherein the substrate is processed both in the electrolytic processing section and in the CMP section.

41. The substrate processing apparatus according to claim 40, wherein the electrolytic processing includes composite electrolytic processing, electrolytic processing using an electrolytic solution, electrolytic processing utilizing a catalyst, and a common electrolytic processing.